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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	12

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,522	NEVILL ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/25/01 to 3/31/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4, 7, 8, 10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 and 24-25 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Pre-Amendment A as received on 6/25/01, Declaration and Fees as received on 10/11/01, IDS as received on 10/11/01, Priority Papers as received on 10/11/01, IDS as received on 11/20/01, Original Declaration as received on 11/20/01, IDS as received on 3/26/03, Change of Address as received on 3/26/03, Change of Address as received on 3/31/04, and IDS as received on 3/31/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The abstract of the disclosure is objected to because of the following informalities:

   a. The abstract contains reference numerals 30, 42, 32 and 62. Because it is an abstract, it is unclear what the reference numerals correspond to. Please remove the reference numerals from the abstract.

b. The abstract contains a line reciting, "[Figure 3]". It is unclear why this phrase is in the abstract, as no figure is present. Please remove the above phrase from the abstract.

Correction is required. See MPEP § 608.01(b).

Claim Objections

6. Claims 16 and 25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

7. Claims 16 recites the limitation, "A computer program product holding a computer program for controlling a computer to perform the method of claim 13". The parent claim of claim 16, claim 1, already claims a processor (processor core) that executes instructions to control it, instructions which inherently reside on some sort of computer readable medium (computer program product). Therefore, because there is no way that the processor core of claim 1 can function as claimed without the instructions that execute on the processor core being comprised on a computer program product, claim 16 fails to further limit the subject matter of claim 1.

8. Claims 25 recites the limitation, "A computer program product holding a computer program for controlling a computer to perform the method of claim 24". The parent claim of claim 25, claim 24, already claims a processor (processor core) that executes instructions to control it, instructions which inherently reside on some sort of computer readable medium

(computer program product). Therefore, because there is no way that the processor core of claim 24 can function as claimed without the instructions that execute on the processor core being comprised on a computer program product, claim 25 fails to further limit the subject matter of claim 24.

9. Claims 1-16 and 17-22 are objected to because of the following informalities:

a. Claim 1 recites the limitation, "Apparatus for processing data" in its preamble. Please amend the claim language to read, "An apparatus for processing data" in order to be more grammatically correct. The same correction needs to also be made for dependent claims 2-14 and 16, as well as for independent claim 17 and its dependent claims 18-22.

b. Claim 8 recites the limitation, "when executing instructions of said second instruction set so and is used to restart execution" on its second and third lines. It is unclear what the word "so" refers to in the claim language. Please amend the claim language to remove the word "so" and thus more clearly define the metes and bounds of the claimed invention.

c. Claim 11 recites the limitation, "said register bank hold stack operands from a top potion of said stack". Please amend the claim language to read, "said register bank holds stack operands from a top portion of said stack" in order to be more grammatically correct.

d. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim that depends from a dependent claim should not be separated by any claim

that does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n). See claims 9-12, where claim 11 improperly depends on claim 10, while claim 12 depends on claim 9. Also see claims 13-16, where claim 16 improperly depends on claim 13, while claim 14 depends on claim 1 and claim 15 is independent.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-16 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 1 recites the limitation, "a plurality of operations that may be specified by instructions". This language is indefinite, as it is unclear if the plurality of operations are specified by instructions of the first instruction set or not. Please amend the claim language to more clearly define the metes and bounds of the claimed invention. See also similar corrections required in claims 15 and 22. Dependent claims 2-14 and 16 are rejected for the same reasons as above, as they include the limitations of their parent claim.

13. Claim 3 recites the limitation, "said translator output signals include control signals that control operation of said processor core and match signals produced on decoding instructions of

said first instruction set". It is unclear whether "match signals" refers to a separate group of signals of the translator output signals simply called "match signals", or if it refers to the "control signals" being equal to signals "produced on decoding instructions of a said first instruction set". Please correct the claim language to more clearly define the metes and bounds of the invention. For the purposes of this examination, the Examiner will assume that "match signals" refer to "control signals" being equal to signals "produced on decoding instruction of a said first instruction set".

14. Claim 16 recites the limitation "the method of claim 13" in its second line. There is insufficient antecedent basis for this limitation in the claim. Claim 13 is directed towards an apparatus, and does not claim any method steps.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 1-8, 10, 13 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Novak et al., U.S. Patent No. 5,909,567.

17. Regarding claim 1, Novak has taught an apparatus for processing data, said apparatus comprising:

a. A processor core (120 of Fig.2) operable to execute operations as specified by instructions of a first instruction set (RISC) (see Col.3 lines 24-26), said processor core having an instruction pipeline (see Fig.2, Fig.5 and Col.2 lines 55-56) into which instructions to be executed are fetched from a memory (214 of Fig.2) and along which instructions progress (see Fig.2, Fig.5 and Col.4 lines 9-20),

b. An instruction translator (220 of Fig.2) operable to translate instructions of a second instruction set (CISC) into translator output signals corresponding to instructions of said first instruction set (see Col.4 lines 10-20). Here, the instruction decoder (220 of Fig.2) outputs both translated instructions in a first instruction set (RISC) (see Col.4 lines 10-20) as well as control signals relating to native (RISC) instructions (see Col.6 lines 1-13).

c. Wherein said instruction translator is within said instruction pipeline (see Fig.2, Fig.5and Col.2 lines 55-56) and translates instructions of said second instruction set that have been fetched into said instruction pipeline from said memory (see Col.4 lines 10-20),

d. At least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of said first instruction set in order to be performed by said processor core (see Col.4 lines 10-17),

e. Said instruction translator (220 of Fig.2) is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation (see Col.4 lines 10-17).

18. Regarding claim 2, Novak has taught an apparatus as claimed in claim 1, wherein said translator output signals include signals forming an instruction of said first instruction set (see Col.4 lines 10-17).

19. Regarding claim 3, Novak has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and match control signals produced on decoding instructions of said first instruction set (see Col.5 lines 30-38). Here, RISC instructions, which are control signals that control the processing core, are the same whether they were translated or not when being passed to the processor core.

20. Regarding claim 4, Novak has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set (see Col.5 lines 30-41). Here, while the RISC instructions that control the processing core are the same for translated and native instructions, there are interrupt control signals that are not specified in native mode that must be specified in non-native mode in order for the CISC instructions to function correctly (see Col.5 line 45 – Col.6 line 24).

21. Regarding claim 5, Novak has taught an apparatus as claimed in claim 1, wherein said processor core fetches instructions from an instruction address within said memory specified by a program counter value held by said processor core (see Col.10 lines 13-34).

22. Regarding claim 6, Novak has taught an apparatus as claimed in claim 5, wherein, when an instruction of said second instruction set is executed, said program counter value is advanced by an amount that is independent of whether or not said instruction of said second instruction set specifies a multi-step operation (see Col.21 lines 6-12). Here, the program counter which

designates CISC instructions (second instruction set) is updated sequentially on every cycle, corresponding to a new CISC instruction, a value that is independent of the multi-step nature of some CISC instructions, as only the translated RISC instructions will be separately addressable.

23. Regarding claim 7, Novak has taught an apparatus as claimed in claim 5, wherein, when an instruction of said second instruction set ("CISC" of Col.6 lines 13-24) is executed, said program counter value is advanced to specify a next instruction of said second instruction set to be executed (see Col.6 lines 13-24).

24. Regarding claim 8, Novak has taught an apparatus as claimed in claim 5, wherein said program counter value is saved if an interrupt occurs when executing instructions of said second instruction set so and is used to restart execution of said instructions of said second instruction set after said interrupt (see Col.5 lines 45-61).

25. Regarding claim 10, Novak has taught an apparatus as claimed in claim 1, wherein said processor has a register bank (290 of Fig.2) containing a plurality of registers and instructions of said first instruction set execute operations upon register operands held in said registers (see Col.6 lines 35-52).

26. Regarding claim 13, Novak has taught an apparatus as claimed in claim 1, further comprising a bypass path within said instruction pipeline such that said instruction translator may be bypassed when instructions of said second instruction set are not being processed (see Col.4 lines 53-56).

27. Regarding claim 15, Novak has taught a method of processing data using a processor core (120 of Fig.2) having an instruction pipeline (see Fig.2, Fig.5 and Col.2 lines 55-56) into which instructions to be executed are fetched from a memory (214 of Fig.2) and along which

instructions progress (see Fig.2, Fig.5 and Col.4 lines 9-20), said processor core being operable to execute operations specified by instructions of a first instruction set (RISC) (see Col.3 lines 24-26), said method comprising the steps of:

a. Fetching instructions into said instruction pipeline,

b. Translating fetched instructions of a second instruction set (CISC) into translator output signals corresponding to instructions of said first instruction set (see Col.4 lines 10-20) using an instruction translator (220 of Fig.2) within said pipeline (see Col.4 lines 10-20). Here, the instruction decoder (220 of Fig.2) outputs both translated instructions in a first instruction set (RISC) (see Col.4 lines 10-20) as well as control signals relating to native (RISC) instructions (see Col.6 lines 1-13).

c. Wherein at least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of said first instruction set in order to be performed by said processor core (see Col.4 lines 10-17),

d. Said instruction translator (220 of Fig.2) is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation (see Col.4 lines 10-17).

28. Regarding claim 16, Novak has taught a computer program product holding a computer program for controlling a computer to perform the method of claim 13 (see Col.3 lines 5-23).

29. Claims 17-19 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Tremblay et al., U.S. Patent No. 6,249,861.

30. Regarding claim 17, Tremblay has taught an apparatus for processing data, said apparatus comprising:

a. A processor core (110/112 of Fig.1) operable to execute operations as specified by instructions of a first instruction set (202 of Fig.2), said processor core having an instruction pipeline into which instructions to be executed are fetched from a memory (106 of Fig.4) and along which instructions progress (see Col.3 lines 34-45, 64-67). Here, the processor cores can execute instructions of a first instruction set, i.e. those that are power-of-two sized (see Col.3 lines 10-24 and Col.4 lines 34-43).

b. An instruction translator (308 of Fig.3) operable to translate instructions of a second instruction set (204 of Fig.2) into translator output signals corresponding to instructions of said first instruction set (see Col.3 lines 10-24, Col.4 lines 40-60 and Col.5 lines 12-20),

c. Wherein said instructions of said second instruction set are variable length instructions (see Col.3 lines 25-33 and Col.4 lines 44-59),

d. Said instruction translator is within said instruction pipeline (see Fig.4) and translates instructions of said second instruction set that have been fetched into a fetch stage of said instruction pipeline from said memory (see Col.4 line 60 – Col.5 line 20),

e. Said fetch stage of said instruction pipeline includes an instruction buffer (306 of Fig.4) holding at least a current instruction word and a next instruction word fetched from said memory such that if a variable length instruction of said second

instruction set starts within said current instruction word and extends into said next instruction word, then said next instruction word is available within said pipeline for translation by said instruction translator without requiring a further fetch operation (see Col.4 line 60 – Col.5 line 12 and Col.5 line 40 – Col.6 line 14).

31. Regarding claim 18, Tremblay has taught an apparatus as in claim 17, wherein said instruction buffer (306 of Fig.4) is a swing buffer (see Col.4 line 60 – Col.5 line 12).

32. Regarding claim 19, Tremblay has taught an apparatus as claimed in claim 17, wherein said fetch stage includes a plurality of multiplexers (602, 604, 606, 608 of Fig.8) for selecting a variable length instruction from one or more of said current instruction word and said next instruction word (see Col.8 lines 32-51).

33. Regarding claim 24, Tremblay has taught a method of processing data using a processor core (110/112 of Fig.1) operable to execute operations as specified by instructions of a first instruction set (202 of Fig.2), said processor core having an instruction pipeline (see Fig.4) into which instructions to be executed are fetched from a memory (106 of Fig.4) and along which instructions progress (see Col.3 lines 34-45, 64-67), said method comprising the steps of:

a. Fetching instructions into said instruction pipeline (see Col.3 lines 34-45, 64-67),

b. Translating fetched instructions of a second instruction set (204 of Fig.2) into translator output signals corresponding to instructions of said first instruction set using an instruction translator (308 of Fig.3) within said instruction pipeline (see Col.3 lines 10-24, Col.4 lines 40-60 and Col.5 lines 12-20),

c. Wherein said instructions of said second instruction set (204 of Fig.2) are variable length instructions (see Col.3 lines 25-33 and Col.4 lines 44-59),

d. Said instruction translator is within said instruction pipeline (see Fig.4) and translates instructions of said second instruction set that have been fetched into a fetch stage of said instruction pipeline from said memory (see Col.4 line 60 – Col.5 line 20),

e. Said fetch stage of said instruction pipeline includes an instruction buffer (306 of Fig.4) holding at least a current instruction word and a next instruction word fetched from said memory such that if a variable length instruction of said second instruction set starts within said current instruction word and extends into said next instruction word, then said next instruction word is available within said pipeline for translation by said instruction translator without requiring a further fetch operation (see Col.4 line 60 – Col.5 line 12 and Col.5 line 40 – Col.6 line 14).

34. Regarding claim 25, Tremblay has taught a computer program product holding a computer program for controlling a computer to perform the method of claim 24 (see Col.3 lines 34-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 9, 11-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Novak et al., U.S. Patent No. 5,909,567 as applied to claims 1 and 10 above, and further in view of Dickol et al., U.S. Patent No. 5,898,885.

36. Regarding claim 9, Novak has taught an apparatus as claimed in claim 1, but has not explicitly taught wherein instructions of said second instruction set specify operations to be executed upon operands held in a stack.

37. However, Dickol has taught non-native Java instructions that specify operations to be executed on operands held in a stack (see Dickol, Col.4 lines 42-61), and those instruction's corresponding translation into RISC-type native instructions so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Novak has taught an apparatus translating instructions from a non-native to a native instruction set (see Novak, Col.4 lines 10-20), but hasn't explicitly specified if the instructions of the non-native (second) instruction set specify operations to be executed on stack operands, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Novak to instead translate instructions specifying operations to be performed on stack operands in a non-native second instruction set into a native first instruction set in a manner so that redundant execution steps are eliminated, thereby improving processor performance.

38. Regarding claim 11, Novak has taught an apparatus as claimed in claim 10, but has not explicitly taught wherein a set of registers within said register bank holds stack operands from a top portion of said stack.

39. However, Dickol has taught wherein a set of registers in a register file hold operands corresponding to a top portion of a stack (see Dickol, Col.2 lines 59-67). Here, when non-native Java paired push and pop instructions are to be translated into native RISC-type instructions, the translation stores those stack operands, which are on the "top" of the stack (due to the LIFO nature of stacks), in the register file, so that unnecessary data transfers are eliminated, and processor performance is improved (see Dickol, Col.4 lines 42-61). Because Novak has taught an apparatus translating instructions from a non-native to a native instruction set (see Novak, Col.4 lines 10-20) with the instructions able to operate on operands in the register file (see Col.6 lines 35-52), but hasn't explicitly specified that the operands in the register file are stack operands, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Novak to instead translate instructions specifying operations to be performed on stack operands in a non-native second instruction set into a native first instruction set in a manner such that redundant stack operations have their operands stored in the register file so that redundant execution steps can be eliminated, thereby improving processor performance.

40. Regarding claim 12, Novak has taught an apparatus as claimed in claim 9, but has not explicitly taught wherein said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said stack, said instruction translator being operable to move between mapping states in dependence upon operations that add or remove stack operands held within said stack.

41. However, Dickol has taught mapping of registers to different stack operands with the ability to move between the mappings based on whether there is a push or a pop operation (see Col.6 lines 27-40), thus allowing non-native to native instruction translation to be executed more

efficiently (see Col.7 lines 5-16). Because Novak has taught an apparatus translating instructions from a non-native to a native instruction set (see Novak, Col.4 lines 10-20), one of ordinary skill in the art would have found it obvious to modify the processor of Novak to map registers of different stack operands with the ability to move between mappings based on if an operation is a push or pop so that non-native to native instruction translation can be executed more efficiently (see Col.7 lines 5-16).

42. Regarding claim 14, Novak has taught an apparatus as claimed in claim 1, but has not explicitly taught wherein said instructions of said second instruction set are Java Virtual Machine bytecodes.

43. However, Dickol has taught non-native Java Virtual Machine instructions being translated into RISC-type native instructions (see Dickol, Col.3 lines 49-57) so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Novak has taught an apparatus translating instructions from a non-native to a native instruction set (see Novak, Col.4 lines 10-20), but hasn't explicitly specified the type of non-native instructions, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Novak to instead translate Java Virtual Machine instructions into a native first instruction set in a manner so that redundant execution steps are eliminated, thereby improving processor performance.

44. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay et al., U.S. Patent No. 6,249,861 as applied to claim 17 above, and further in view of Dickol et al., U.S. Patent No. 5,898,885.

45. Regarding claim 20, Tremblay has taught an apparatus as claimed in claim 17, but has not explicitly taught wherein said instructions of said second instruction set are Java Virtual Machine bytecodes.

46. However, Dickol has taught non-native Java Virtual Machine instructions being translated into RISC-type native instructions (see Dickol, Col.3 lines 49-57) so that redundant execution steps are eliminated and native code execution performance is improved (see Dickol, Col.2 lines 17-39). Because Tremblay has taught an apparatus translating instructions from a non-native to a native instruction set (see Tremblay, Col.3 lines 10-24, Col.4 lines 40-60 and Col.5 lines 12-20), but hasn't explicitly specified the type of non-native instructions, one of ordinary skill in the art would have found it obvious to modify the translation apparatus of Tremblay to instead translate Java Virtual Machine instructions into a native first instruction set in a manner so that redundant execution steps are eliminated, thereby improving processor performance.

47. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay et al., U.S. Patent No. 6,249,861 as applied to claim 17 above, and further in view of Novak et al., U.S. Patent No. 5,909,567.

48. Regarding claim 21, Tremblay has taught an apparatus as claimed in claim 17, but has not explicitly taught the apparatus further comprising a bypass path within said instruction pipeline such that said instruction translator may be bypassed when instructions of said second instruction set are not being processed.

49. However, Novak has taught a bypass path around the instruction translator so native instructions can be passed directly to the processor without going through the time consuming

translation process (see Col.1 lines 43-46), thereby improving system performance (see Novak, Col.4 lines 53-56). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Tremblay to include a bypass path around the instruction translator so that the instruction translator can be bypassed when it is not in use and thus increase processor performance.

50. Regarding claim 22, Tremblay has taught an apparatus as claimed in claim 17, but has not explicitly taught wherein:

a. At least one instruction of said second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of said first instruction set in order to be performed by said processor core,

b. Said instruction translator is operable to generate a sequence of translator output signals to control said processor core to perform said multi-step operation.

51. However, Novak has taught the translation of one instruction in a non-native (second) instruction set into multiple instructions of a native (first) instruction set that execute on (and control) the processor (see Novak, Col.4 lines 10-17) so that overall system performance of non-native instructions on a native instruction set processor can be improved by executing the architecturally superior and more efficient native instructions (see Col.1 lines 12-42). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Tremblay to have a non-native instruction be translated into multiple native instructions to improve the overall system performance on a native instruction set processor.

Conclusion

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

53. Patel et al., U.S. Patent No. 6,332,215, has taught a Java hardware accelerator that translates Java bytecode instructions into native CPU instructions.

54. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

55. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
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